

3. A semiconductor device according to claim 2, wherein the openings are disposed about a center portion of the bonding surface of the bond pad so the center portion of the bonding surface is free of openings.

4. A semiconductor device according to claim [4] 2, wherein the openings comprise a pattern of radiating channels disposed about a center of the bonding surface.

5. A semiconductor device according to claim 2, wherein the openings comprise a series of spaced apart rectangular channels arranged parallel to one another.

6. A semiconductor device according to claim 2, wherein the openings comprise an array of L shaped channels disposed about a center of the bonding surface.

7. A semiconductor device according to claim 2, wherein the openings comprise an array of holes disposed about the bonding surface.

8. A semiconductor device, which comprises:

- a. an active circuit in the semiconductor device;
- b. a wiring pattern overlying and in electrical contact with the active circuit;
- c. bond pads formed as select areas on the wiring pattern; and
- d. a plurality of openings extending [partially] into a substantially flat bonding surface of the bond pads.

9. A semiconductor device according to claim 8, wherein the openings are disposed about a center portion of the bonding surface of the bond pad so that the center portion of the bonding surface is free of openings.

10. A semiconductor device according to claim 8, wherein the openings comprise a pattern of radiating channels disposed about a center of the bonding surface.

11. A semiconductor device according to claim 8, wherein the openings comprise a series of spaced apart rectangular channels arranged parallel to one another.

12. A semiconductor device according to claim 8, wherein the openings comprise an array of L shaped channels disposed about a center of the bonding surface.

13. A semiconductor device according to claim 8, wherein the openings comprise an array of holes disposed about the bonding surface.

14. A semiconductor device according to claim 8, further comprising a passivation layer overlying the wiring pattern, the passivation layer having holes therethrough to expose the bonding surface of the bond pads to enable electrical connection to the bond pads through the holes.

15. A semiconductor device according to claim 8, further comprising bond wires bonded to the bonding surface of the bond pads.

16. A semiconductor device, comprising:

- a. a layer of insulating material;
- b. a substantially flat layer of conductive material over lying the layer of insulating material;
- c. bond pads formed as select areas on a surface of the layer of conductive material; and
- d. at least one opening extending [partially into] through the bond pads.

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17. An improved bond pad comprising:
a metal layer having a substantially planar surface, said metal layer electrically
connected to an active circuit of a semiconductor device and having at least one opening
extending therethrough.
18. An improved bond pad according to claim 17, further comprising a plurality of
openings in the metal layer of the bond pad.
19. An improved bond pad according to claim 18, wherein the openings are
disposed about a center portion of the planar surface of the bond pad so that the center portion
of the planar surface is free of openings.
20. An improved bond pad according to claim 18, wherein the openings comprise a
pattern of radiating channels disposed about a center of the bond pad.
21. An improved bond pad according to claim 18, wherein the openings comprise a
series of spaced apart rectangular channels arranged parallel to one another.
22. An improved bond pad according to claim 18, wherein the openings comprise
an array of L shaped channels disposed about a center of the bond pad.
23. An improved bond pad according to claim 18, wherein the openings comprise
an array of holes disposed about the bond pad.
24. An improved bond pad according to claim 18, further comprising a passivation
layer overlying the metal layer, the passivation layer having holes therethrough to expose the
planar surface of the bond pad to enable electrical connection to the bond pad.
25. An improved bond pad according to claim 18, further comprising a bond wire
bonded to the planar surface of the bond pad.
26. An improved bond pad according to claim 18, wherein said metal layer is
aluminum.
27. [A semiconductor device having an improved bond pad, the semiconductor
device comprising:
a bond pad electrically connected to an active circuit of the semiconductor device, said
bond pad having a substantially planar surface; and
at least one opening extending through said bond pad.

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28. A semiconductor device having an improved bond pad, the bond pad having a metal layer, said metal layer having a substantially planar surface connected to an active circuit of a semiconductor device further having at least one opening extending therethrough, the semiconductor device made according to the method comprising:

forming a thick insulating layer over active circuitry of a semiconductor chip;
etching said thick insulating layer thereby forming clear contact paths to said active circuitry of the semiconductor chip;
forming a metal layer over said thick insulating layer; and
etching said metal layer thereby forming an interconnect wiring pattern and bond pads having at least one opening extending therethrough.

29. A semiconductor device according to claim 27, the method further comprising:
forming a passivation layer over the metal layer; and
etching said passivation layer to expose select areas of the wiring pattern and bond pads.]

add
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